Application No. 09/775,477

REMARKS

Claims 1-218 are pending in the case. Original Claims 63-110 are amended to correct inaccuracies in Claim number and Claim dependency. New Claims 111-218 are fully supported by, and within the scope of, the Specification. No new matter is introduced into the Application by the amended Claims or by the new Claims.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "**Version with markings to show changes made**."

Applicants believe that the Claims pending in the case are in condition for allowance, and an early notice of allowability is respectfully solicited. If the Examiner believes that a telephone conference with Applicant's attorney might expedite prosecution of the application, he is invited to call at the telephone number indicated below.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

~~61~~ 63. (Amended) The memory module of Claim ~~48~~ 58, wherein the memory module is disposed in one of a semiconductor device, an optical device, and a combination thereof.

~~62~~ 64. (Amended) The memory module of Claim ~~48~~ 58, wherein the memory module is embedded in a communication device.

~~63~~ 65. (Amended) A hierarchical memory structure, comprising:

a. memory cells having respective memory states;

b. local sense amplifiers selectively coupled with the memory cells, selected ones of the local sense amplifiers sensing the respective memory states and producing respective local memory state signals representative thereof, wherein the local sense amplifiers produce limited swing voltage signals;

c. local wordline decoders selectively coupled with the memory cells, selected ones of the local wordline decoders selecting respective memory cells responsive to a corresponding local selection signal;

~~c~~ d. global sense amplifiers, selected ones of the global sense amplifiers being coupled with local sense amplifiers, selected ones of the local sense amplifiers being coupled with respective memory cells, selected others of the global sense amplifiers being coupled with the selected ones such that the selected ones of the global sense amplifiers are local sense amplifiers relative to the selected others of the global sense amplifiers in a multi-tiered hierarchy, each local sense amplifier producing a respective local memory state signal to which a corresponding global sense amplifier is responsive;

~~d~~ e. global wordline decoders, selected ones of the global wordline decoders being coupled with respective local wordline decoders, selected others of the global wordline decoders being

coupled with the selected ones such that the selected ones are local wordline decoders relative to the selected others in a multi-tiered hierarchy, each global wordline decoder producing a respective global selection signal to which corresponding local wordline decoders are responsive;

~~e~~ f. one of a single-ended sense amplifier having sample-and-hold reference, and a charge-share limited-swing-driver sense amplifier;

~~f~~ g. an asynchronously-resettable decoder;

~~g~~ h. a wordline decoder having a first memory row and a second memory row coupled therewith, the wordline decoder decoding the first memory row, and being disposed to select and decode the second memory row responsive to an alternative-row-select signal;

~~h~~ i. with the memory module having a designated group of memory cells assigned to represent a logical portion of the memory structure, a redundancy device, including:

(1) a redundant group of memory cells; and

(2) a redundancy controller coupled with the designated group and the redundant group, the redundancy controller assigning the redundant group to the logical portion of the memory structure, responsive to a preselected memory group condition,

wherein each of the designated group and the redundant group comprises one of a memory row, a memory column, a preselected portion of a memory module, a selectable portion of a memory module, a memory module, and a combination thereof;

~~i~~ j. one of a diffusion replica delay circuit and a high-precision delay measurement circuit constraining a limited voltage swing signal; and

~~j~~ k. a data transfer bus circuit coupling a selected one of the global sense amplifiers, local sense amplifiers, global wordline

decoders, and local wordline decoders to a data bus, the circuit imposing a limited voltage swing on the data bus.

~~63~~ 66. (Amended) The memory module of Claim ~~62~~ 65, wherein the hierarchical memory structure is disposed in one of a semiconductor device, an optical device, and a combination thereof.

~~64~~ 67. (Amended) The memory module of Claim ~~62~~ 65, wherein the hierarchical memory structure is embedded in a communication device.

~~65~~ 68. (Amended) A method for substantially simultaneously retrieving a first datum from a first memory location and storing a second datum in a second memory location, wherein both locations are disposed within a single-port hierarchical memory structure having local and global data sensing, and local and global location selecting, the method comprising:

a. locally selecting the first memory location from which the first datum is to be retrieved;

b. locally sensing the first datum (READ operation);

c. globally selecting the second memory location;

d. substantially concurrently with the globally selecting, globally sensing the first datum at the first memory location;

e. outputting the first data subsequent to the globally sensing;

f. inputting the second datum substantially immediately subsequent to the outputting the first datum;

g. locally selecting the second memory location; and

h. storing the second datum (WRITE operation).

~~66~~ 69. (Amended) The method of Claim ~~65~~ 68, further comprising precharging bitlines coupled with the first and the second

memory locations, prior to locally sensing the first datum (PRECHARGE operation).

~~67~~ 70. (Amended) The method of Claim ~~65~~ 68, wherein (a) through (h) are completed within one access cycle of the memory structure.

~~68~~ 71. (Amended) The method of Claim ~~66~~ 69, wherein a plurality of PRECHARGE-READ-WRITE operations are completed within one access cycle of the memory structure.

~~69~~ 72. (Amended) A method for providing sequential storage of a first datum in a first hierarchical memory structure location and a second datum in a second hierarchical memory structure location within one access cycle of the memory structure, the structure having local and global location selecting, the method comprising:

a. globally selecting the first hierarchical memory structure location to which the first datum is to be stored;

b. precharging bitlines coupled with the memory cells at the first hierarchical memory structure location (PRECHARGE1 operation);

c. locally selecting the first hierarchical memory structure location;

d. storing the first datum (WRITE1 operation);

e. globally selecting the second hierarchical memory structure location to which the second datum is to be stored;

f. substantially concurrently with the globally selecting the second hierarchical memory structure location, precharging bitlines coupled with the second hierarchical memory structure location (PRECHARGE2 operation);

g. locally selecting the second hierarchical memory structure location; and

h. storing the second datum (WRITE2 operation).

~~70~~ 73. (Amended) A hierarchical memory structure comprising:

a. memory cells;

b. sense amplifiers coupled with the memory cells to form memory columns; and

c. decoders coupled with the memory cells to form memory rows,

wherein the memory cells, sense amplifiers, and decoders so coupled form a first tier memory module, and at least one of the first tier sense amplifiers and the first tier decoders provide a limited swing voltage signal.

~~71~~ 74. (Amended) Thee hierarchical memory structure of Claim ~~70~~ 73, further comprising:

a. *(n-1)*-tier memory modules;

b. *(n)*-tier sense amplifiers coupled with the *(n-1)*-tier sense amplifiers in the *(n-1)*-tier memory modules; and

c. *(n)*-tier decoders coupled with the *(n-1)*-tier decoders in the *(n-1)*-tier memory modules,

wherein n > 1, and wherein the *(n-1)*-tier memory modules, *(n)*-tier sense amplifiers, and *(n)*-tier decoders so coupled form an *(n)*-tier memory module.

~~72~~ 75. (Amended) The hierarchical memory structure of Claim ~~71~~ 74, wherein one of the *(n)*-tier sense amplifiers, *(n-1)*-tier sense amplifiers, *(n)*-tier decoders, and *(n-1)*-tier decoders produces a limited swing voltage signal.

~~73~~ 76. (Amended) The hierarchical memory structure of Claim ~~71~~ 74, wherein one of the *(n)*-tier sense amplifiers, *(n-1)*-tier sense

amplifiers, *(n)*-tier decoders, and *(n-1)*-tier decoders is responsive to a limited swing voltage signal.

~~74~~ 77. (Amended) The hierarchical memory structure of Claim ~~72~~ 75, wherein one of the *(n)*-tier sense amplifiers, *(n-1)*-tier sense amplifiers, *(n)*-tier decoders, and *(n-1)*-tier decoders is responsive to a limited swing voltage signal.

~~75~~ 78. (Amended) The hierarchical memory structure of Claim ~~70~~ 73, wherein one of plurality of first tier decoders is an asynchronously resettable row decoder.

79. (Amended) The hierarchical memory structure of Claim 73, further comprising one of a redundant memory row and a redundant memory column.

80. (Amended) The hierarchical memory structure of Claim 74, wherein a selected one of the pluralities of *(n)*-tier sense amplifiers and *(n-1)*-tier sense amplifiers is one of a single-ended sense amplifier having sample-and-hold reference, and a charge-share limited-swing-driver sense amplifier.

~~78~~ 81. (Amended) The hierarchical memory structure of Claim ~~70~~ 73, further comprising a row decoder having a first memory row and a second memory row coupled therewith, the row decoder decoding the first memory row, and being disposed to select and decode the second memory row responsive to an alternative-row-select signal.

~~79~~ 82. (Amended) The hierarchical memory structure of Claim ~~78~~ 81, further comprising a row decoder having an assigned memory row and a redundant memory row coupled therewith, the row decoder decoding the assigned memory row, and being disposed to select and

decode the redundant memory row responsive to a redundant-row-select signal.

~~80~~ 83. (Amended) The hierarchical memory structure of Claim ~~75~~ 78, the asynchronously-resettable row decoder having a first memory row and a second memory row coupled therewith, the row decoder decoding the first memory row, and being disposed to select and decode the second memory row responsive to an alternative-row-select signal.

~~81~~ 84. (Amended) The hierarchical memory structure of Claim ~~72~~ 75, wherein one of the *(n)*-tier sense amplifiers and *(n-1)*-tier sense amplifiers is one of a single-ended sense amplifier having sample-and-hold reference, and a charge-share limited-swing-driver sense amplifier.

~~82~~ 85. (Amended) The hierarchical memory structure of Claim ~~81~~ 84, wherein a second selected one of the pluralities of *(n)*-tier sense amplifiers, *(n-1)*-tier sense amplifiers, *(n)*-tier decoders, and *(n-1)*-tier decoders is responsive to a limited swing voltage signal.

~~83~~ 86. (Amended) The hierarchical memory structure of Claim ~~81~~ 84, wherein one of the decoders is an asynchronously resettable row decoder.

~~84~~ 87. (Amended) The hierarchical memory structure of Claim ~~83~~ 86, further comprising a row decoder having a first memory row and a second memory row coupled therewith, the row decoder decoding the first memory row, and being disposed to select and decode the second memory row responsive to an alternative-row-select signal.

~~85~~ 88. (Amended) The hierarchical memory structure of Claim ~~83~~ 86, wherein the asynchronously-resettable row decoder is coupled

with a first memory row and a second memory row, the row decoder decoding the first memory row, and being disposed to select and decode the second memory row responsive to an alternative-row-select signal.

~~86~~ 89. (Amended) The hierarchical memory structure of Claim ~~83~~ 86, further comprising one of a redundant memory row and a redundant memory column.

~~87~~ 90. (Amended) The hierarchical memory structure of Claim ~~86~~ 89, further comprising a row decoder having an assigned memory row and a redundant memory row coupled therewith, the row decoder decoding the assigned memory row, and being disposed to select and decode the redundant memory row responsive to a redundant-row-select signal.

~~88~~ 91. (Amended) The hierarchical memory structure of Claim ~~71~~ 74, having a designated group of memory cells assigned to represent a logical portion of the memory structure, the structure further comprising:

a. a redundant group of memory cells; and

b. a redundancy controller coupled with the designated group and the redundant group, the redundancy controller assigning the redundant group to the logical portion of the memory structure, responsive to a preselected memory group condition.

~~89~~ 92. (Amended) The hierarchical memory structure of Claim ~~88~~ 91, wherein the redundancy controller comprises a redundancy decoder responsive to an encoded signal representative of the preselected memory group condition.

~~90~~ 93. (Amended) The hierarchical memory structure of Claim ~~89~~ 92, wherein the redundancy controller further comprises a plurality

of selectable switches, the plurality of selectable switches encoding the preselected memory group condition.

~~91~~ 94. (Amended) The hierarchical memory structure of Claim ~~90~~ 93, wherein the plurality of selectable switches are fuses.

~~92~~ 95. (Amended) The hierarchical memory structure of Claim ~~90~~ 93, wherein the preselected memory group condition is a "FAILED" memory group condition, representative of a designated group malfunction.

~~93~~ 96. (Amended) The hierarchical memory structure of Claim ~~88~~ 91, wherein each of the designated group and the redundant group comprise one of a memory row, a memory column, a preselected portion of a memory module, a selectable portion of a memory module, a memory module, and a combination thereof.

~~94~~ 97. (Amended) The hierarchical memory structure of Claim ~~72~~ 75, further comprising a limited swing voltage driver circuit constraining the limited swing voltage signal.

~~95~~ 98. (Amended) The hierarchical memory structure of Claim ~~72~~ 75, further comprising a high-precision delay measurement circuit constraining the limited swing voltage signal.

~~96~~ 99. (Amended) The hierarchical memory structure of Claim ~~95~~ 98, wherein the high-precision delay measurement circuit comprises a ring oscillator executing oscillation cycle in a predefined oscillation period.

~~97~~ 100. (Amended) The hierarchical memory structure of Claim ~~96~~ 99, wherein the ring oscillator executes a plurality of oscillation

cycles by circulating an oscillation signal therein, and the ring oscillator comprises:

a. a plurality of oscillator stages; and

b. a plurality of oscillation signal detectors interposed between selected ones of the oscillator stages, the plurality of oscillation signal detectors detecting the location of the oscillation signal within the ring oscillator during a measured oscillation cycle, responsive to a measurement signal.

~~98~~ 101. (Amended) The hierarchical memory structure of Claim ~~97~~ 100, wherein the high-precision delay measurement circuit further comprises a counter coupled with the ring oscillator, an oscillator cycle incrementing the counter, and the counter measuring cardinality of the plurality of oscillation cycles thereby.

~~99~~ 102. (Amended) The hierarchical memory structure of Claim ~~98~~ 101, wherein the oscillation signal has alternating positive signal edges and negative signal edges on successive ones of the plurality of oscillation cycles, and wherein the high-precision delay measurement circuit further comprises a positive edge counter and a negative edge counter, each of the positive edge counter and the negative edge counter measuring cardinality of the plurality of oscillation cycles.

~~100~~ 103. (Amended) The hierarchical memory structure of Claim ~~99~~ 102, wherein the plurality of oscillation counters comprise a dual-edge detection counter.

~~101~~ 104. (Amended) The hierarchical memory structure of Claim ~~72~~ 75, further comprising a diffusion replica delay circuit constraining the limited voltage swing signal.

~~102~~ 105. (Amended) The hierarchical memory structure of Claim ~~101~~ 104, wherein the diffusion replica delay circuit comprises dummy cells operably coupled with a selected wordline decoder and a selected sense amplifier.

~~103~~ 106. (Amended) The hierarchical memory structure of Claim ~~102~~ 105, wherein the dummy cells comprise split dummy bit lines.

~~104~~ 107. (Amended) The hierarchical memory structure of Claim ~~71~~ 74, further comprising a data transfer bus circuit coupling a selected one of the pluralities of global sense amplifiers, local sense amplifiers, global wordline decoders, and local wordline decoders to a data bus, the circuit imposed a limited voltage swing on the data bus.

~~105~~ 108. (Amended) The hierarchical memory structure of Claim ~~104~~ 107, wherein the data transfer bus circuit comprises a programmable driver programmed to impose logic signals on the data bus.

~~106~~ 109. (Amended) The hierarchical memory structure of Claim ~~105~~ 108, wherein the programmable driver is programmed to impose encoded signals on the data bus.

~~107~~ 110. (Amended) The hierarchical memory structure of Claim ~~105~~ 108, wherein the programmable driver is programmed to impose multilevel logic signals on the data bus.